Trap Read Only Non-Volatile Memory (TROM)

ABSTRACT

[0046] A Trap Read Only Memory (TROM) architecture employs a NAND-type array structure configured as a read-only memory that is programmed only one time. The memory cells in the array comprise a gate terminal, a first channel terminal (source/drain), a second channel terminal (drain/source) and a channel region between the first and second channel terminals. A charge trapping structure, such as a layer of silicon nitride, is formed over the channel region. A tunneling dielectric is placed between the channel region and the charge trapping structure, and a blocking dielectric is placed between the charge trapping structure and the gate terminal. An E-field assisted (Fowler-Nordheim FN) tunneling program algorithm is applied.